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H04L 25/02

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WO 94/22252 A1 WO 92/02085 A1 US 5206888 A
US 5072407 A US 3909724 A

(58) Field of Search
UK CL (Edition O) H4P PDRX PEM
INT CL^6 H04L 25/02
ONLINE:WPI

(54) Abstract Title

A modem in which bit rate is determined using the width of a start bit

(57) A modem (102) having circuit for detecting a bit rate using a start bit. The circuit comprises a microcontroller (202), a Universal Asynchronous Receiver Transmitter (UART) (204), and a clock generator and counter (206). The UART (204) and the clock generator and counter (206) are both coupled to the microcontroller (202). The clock generator and counter (206) has a clock and a counter, the clock being arranged to run at a speed greater than the bit rate. The counter determines the width of the start bit. The microcontroller is arranged to determine the bit rate using the speed of the clock and the width of the start bit.

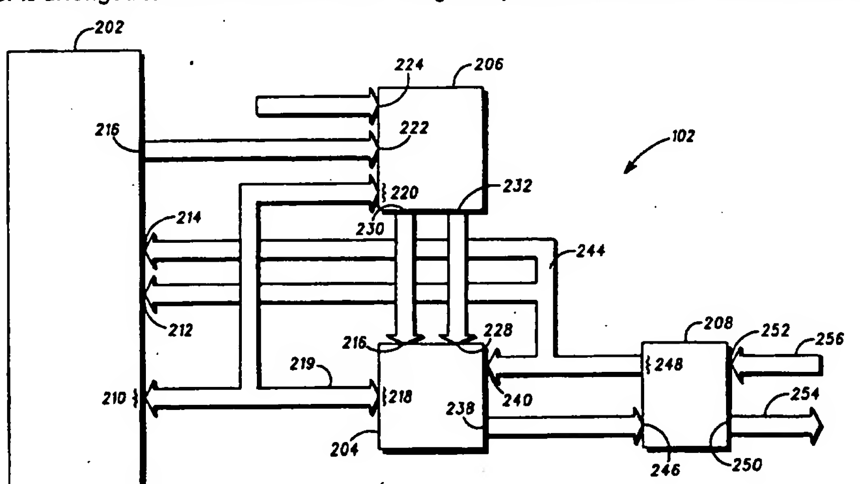

FIG.2

GB 2 324 688 A

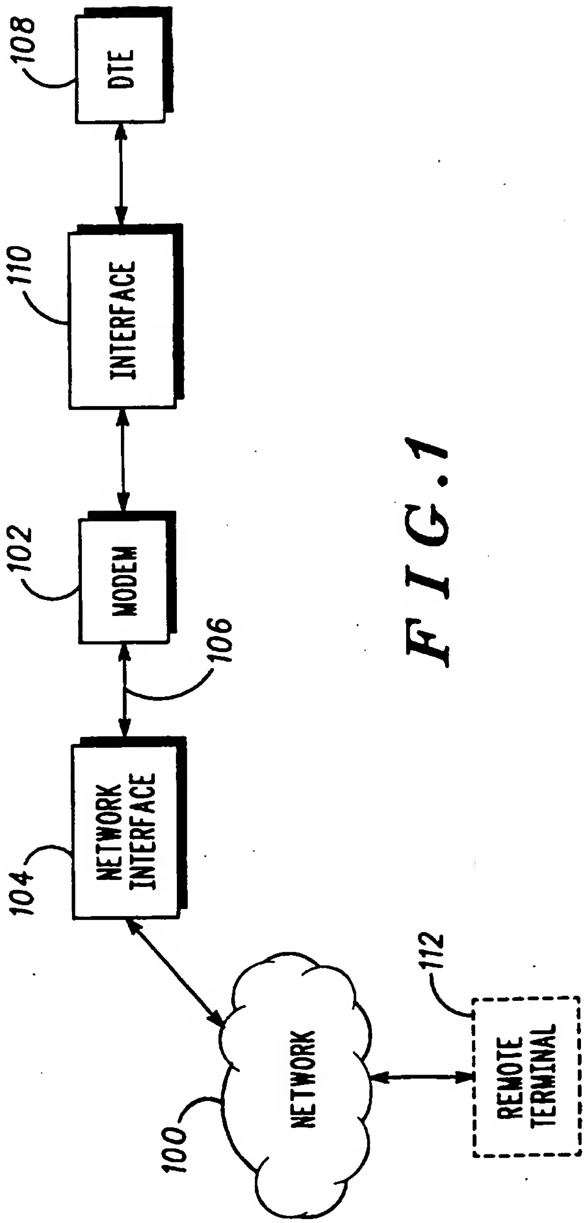
108
DTE
110
INTERFACE
102
MODEM
106
104
NETWORK
INTERFACE
100
NETWORK
112
REMOTE
TERMINAL

FIG.1

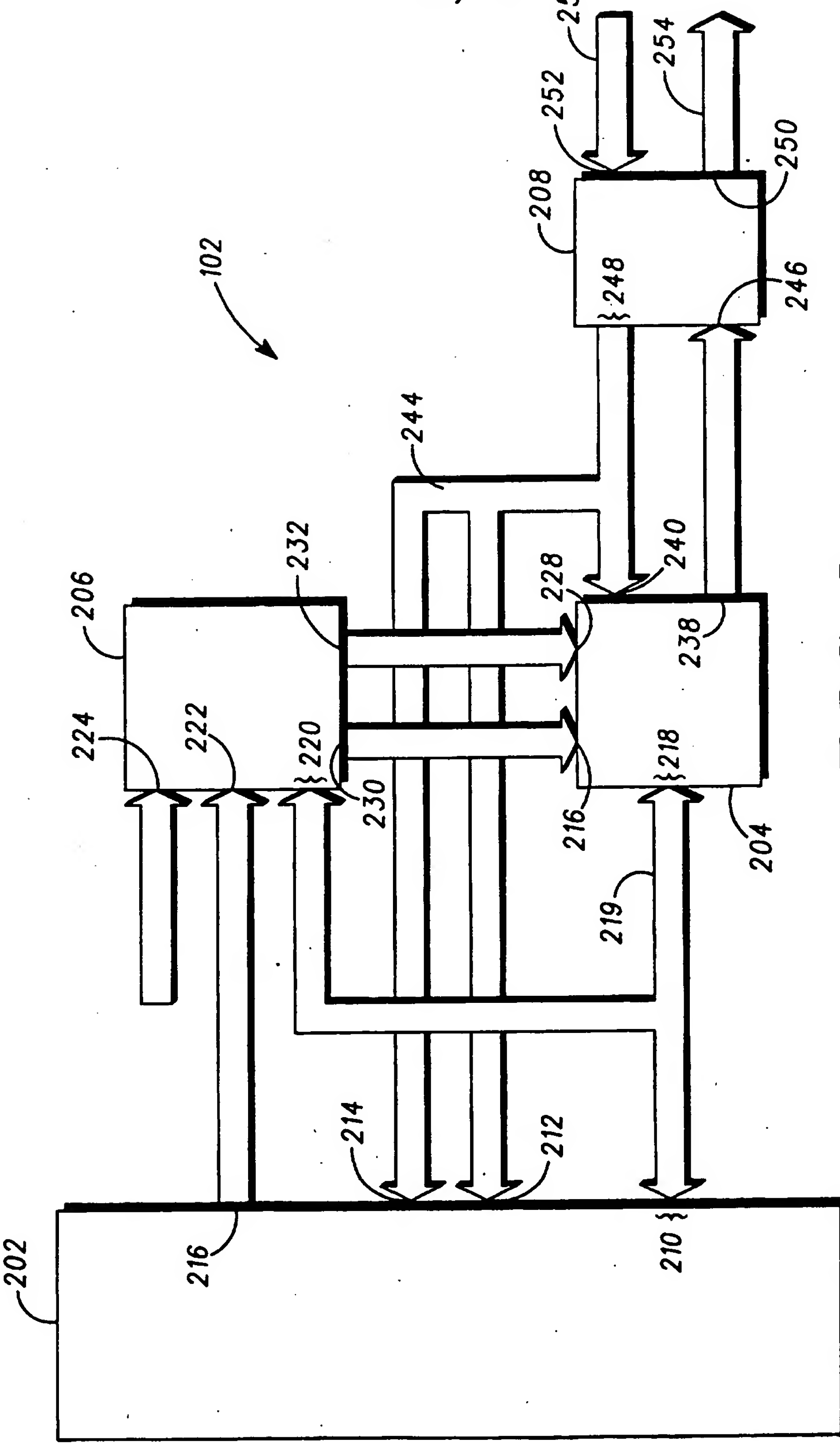
102
202
204
206
208
210
212
214
216
218
219
220
222
224
228
230
232
238
240
244
246
248
250
252
254
256

FIG. 2

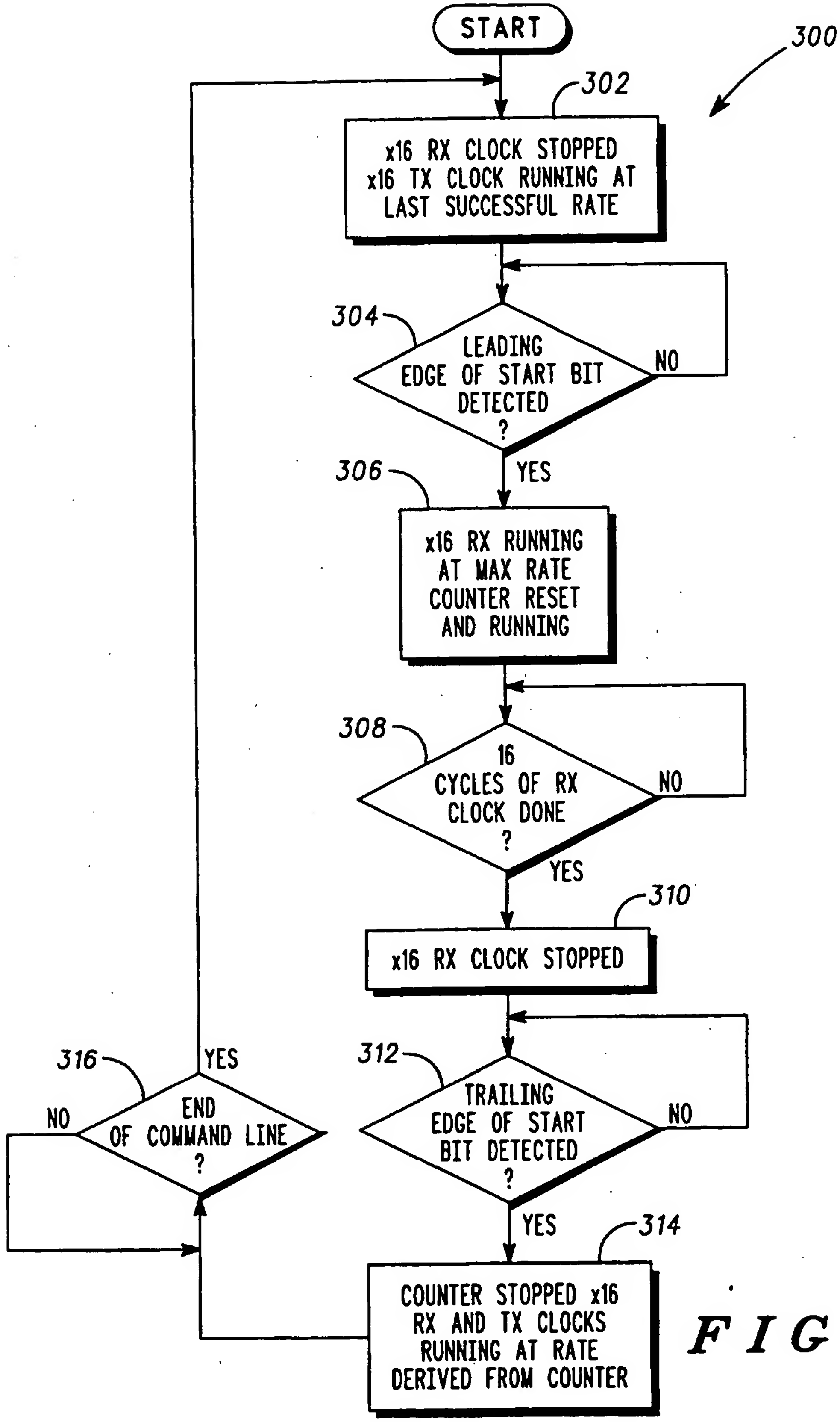
START
300
302
x16 RX CLOCK STOPPED
x16 TX CLOCK RUNNING AT
LAST SUCCESSFUL RATE
304
LEADING
EDGE OF START BIT
DETECTED
?
NO
306
YES
x16 RX RUNNING
AT MAX RATE
COUNTER RESET
AND RUNNING
308
16
CYCLES OF RX
CLOCK DONE
?
NO
YES
310
x16 RX CLOCK STOPPED
316
YES
END
OF COMMAND LINE
?
NO
312
TRAILING
EDGE OF START
BIT DETECTED
?
NO
YES
314
COUNTER STOPPED x16
RX AND TX CLOCKS
RUNNING AT RATE
DERIVED FROM COUNTER

FIG.3

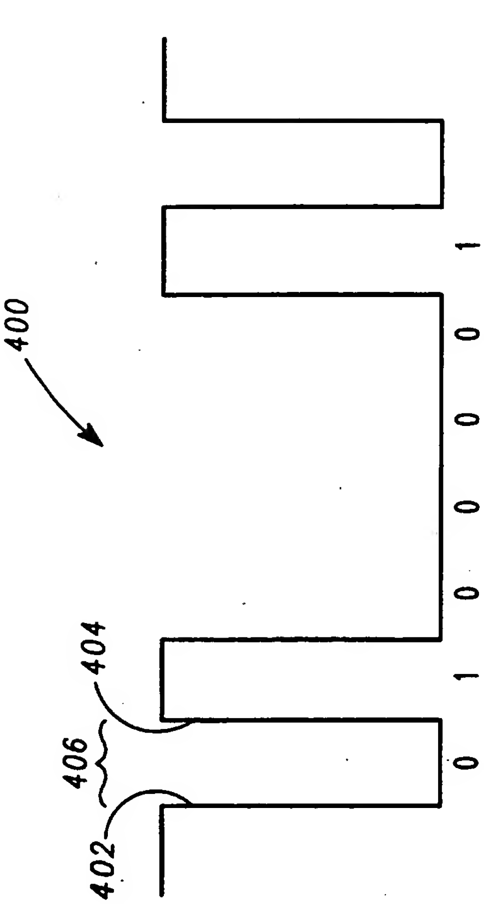

FIG. 4

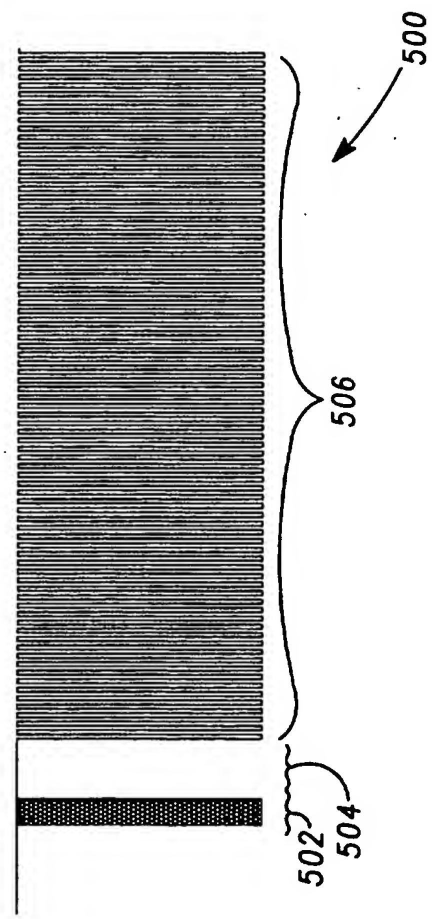

FIG. 5

AN APPARATUS FOR AND METHOD OF DETECTING A BIT RATE

Field of the Invention

The present invention relates to an apparatus for and method of detecting a bit rate for use with communications equipment, for example, a modem.

Background of the Invention

Autobauding, or the automatic detection of a bit rate, is a technique for automatic detection of a bit rate in a digital communications system and relieves the user of having to configure a Data Terminating Equipment (DTE), for example, a terminal, to communications link parameters of a Data Communications Equipment (DCE), such as a modem. The parameters to be determined are: speed, parity and stop bits.

The industry standard method for autobauding requires that a command line sent via the communications link to the DCE be prefixed with the American Standard Code for Information Interchange (ASCII) characters 'A' and 'T'. By examining the bits constituting these characters, the above parameters can be determined by the DCE.

In particular, a microprocessor under software control measures the width of a start bit of the 'A' and then scans the remainder of the bits constituting the 'A' by sampling the received data at the nominal centre of each subsequent bit constituting the 'A'. Detection of the 'A' in this way allows a Universal Asynchronous Receiver Transmitter (UART) to be configured to capture the rest of the command line.

However, autobauding in this way requires dedicated processing power or specific hardware assistance. In a single processor multi-tasking environment, this is disadvantageous for two reasons. Firstly, if the DTE is running at a speed in excess of 38400 bits per second, it is difficult to measure the width of the start bit accurately, since the speed of the processor is typically too slow to detect the beginning of the start bit. Secondly, if the bit rate is slow, for example, less than 9600 bits per second

for a given processor, it is unacceptable to monopolise the processor for the entire duration of the transmission of the 'A'.

Therefore, an object of the present invention is to obviate or mitigate the above mentioned problems associated with autobauding.

Statement of Invention

According to the present invention, there is provided an apparatus for detecting a bit rate using a start bit, comprising a processor, communicating means coupled to the processor, a clock arranged to run at a speed greater than the bit rate, and a counter for determining the width of the start bit, the clock and the counter being coupled to the processor, wherein the processor is arranged to determine the bit rate using the speed of the clock and the width of the start bit.

In a preferred embodiment, the communicating means is a universal asynchronous receiver transmitter, and the processor is arranged to detect a leading edge of the start bit. The processor may be arranged to detect a trailing edge of the start bit.

Preferably, operation of the clock is selective and the counter is synchronised to the clock.

The communicating means may have a maximum bit rate and the clock may be arranged to run a predetermined number of times faster than the maximum bit rate. Preferably, the predetermined number of times is sixteen. Conveniently, the clock is arranged to run for a predetermined number of cycles. The predetermined number of cycles may be sixteen. The clock may be arranged to generate a transmit clock signal and a receive clock signal from a master clock signal. Preferably, the receive clock signal is a factor of the master clock signal.

The processor may have a bit port for sensing data polarity and the processor may be arranged to generate an interrupt in response to the start bit.

The receive clock signal may be halted, the transmitter clock signal may be enabled, and the clock and the counter may be initialised.

According to the present invention, there is also provided a method of detecting a bit rate using a start bit, comprising the steps of: starting a clock and a counter in response to a characteristic of the start bit, the clock being arranged to run at a speed greater than the bit rate, determining the width of the start bit using the counter, determining the bit rate using the speed of the clock and the width of the start bit.

In a preferred embodiment, the start bit is a leading edge of the start bit.

The method may comprise the step of running the clock a predetermined number of times faster than the bit rate. Preferably, the predetermined number of times is sixteen.

The method may further comprise the step of running the clock for a predetermined number of cycles. Preferably, the predetermined number of cycles is sixteen.

Conveniently, the method further comprises the step of generating a receive clock signal and a transmit clock signal from a master clock.

A processor interrupt may be generated in response to the start bit.

It is thus possible to provide an apparatus and method which can accurately determine the bit rate of a command line whilst conserving processor resources, i.e. the bit rate can be determined solely from the start bit and so the processor resources are only required for the duration of the start bit, rather than the whole of the character 'A'. The autobauding process therefore becomes a background process and is virtually invisible to other foreground tasks. This means that any standard library software routines used to send and receive data from the UART do not have any interaction with the autobauding process.

Brief Description of the Drawings

The invention will now be described in more detail, by way of example, with reference to the accompanying drawings, in which:

FIG. 1 is a schematic diagram of an apparatus arrangement constituting an embodiment of the invention,

FIG. 2 is a schematic diagram of an apparatus constituting an embodiment of the invention,

FIG. 3 is a flow diagram of a method for the apparatus of FIG. 2,

FIG. 4 is a portion of a command line which may be used with the method of FIG. 3, and

FIG. 5 is a schematic representation of a clock signal constituting an embodiment of the present invention.

Description of a Preferred Embodiment

Referring to FIG. 1, a Data Terminating Equipment (DTE) 108 is connected via an interface 110 to a modem 102 having a maximum autobaud rate. The modem 102 is connected to a telephone network interface 104 via a cable 106, the interface 104 being connected to a telephone network 100. A remote DTE 112 is also connected to the network 100 in a similar manner.

The modem 102 (FIG. 2) includes a microcontroller 202, a communicating means, for example, a UART 204, a clock generator and counter 206 (hereinafter referred to as a "generator") and a V.28 transceiver 208.

The microcontroller 202 has a control bus port 210, a single bit port 212 for sampling data received, an interrupt port 214, and a reset counter terminal 216.

The control bus port 210 is connected to a corresponding control bus port 218 of the UART 204 and a corresponding control bus port 220 of the generator

206 via a control bus 219. The single bit port 212 and the interrupt port 214 are both connected to a first output port 248 of the transceiver 208 and a data input port 240 of the UART 204, via a data bus 244. The reset counter terminal 216 is connected to a corresponding reset terminal 222 of the generator 206 for resetting a counter (not shown).

The generator 206 has a clock signal input terminal 224 for receiving a master clock signal from a master clock (not shown). The generator 206 is capable of generating a transmit clock signal and a receive clock signal, both of which can be set to a multiple of up to sixteen times a maximum autobaud rate of the modem 102. The generator 206 has a transmit clock output port 230 and a receive clock output port 232 connected to a transmit clock input port 226 and a receive clock input port 228 of the UART 204, respectively.

The transceiver 208 has a first input port 246 connected to an output data port 238 of the UART 204. The transceiver 208 is also connected to a data output line 254 and a data input line 256 via a second output port 250 and a second input port 252, respectively.

All of the above described elements are, but do not necessarily have to be, contained within a RUBY ASIC. This is an Advanced RISC (Reduced Instruction Set Chip) Machine based on an Application Specific Integrated Circuit produced by VLSI Technology, Inc., under part number VPS10101-3.

During normal operation, data is transmitted and received by the transceiver 208 at the second output port 250 and the second input port 252, respectively, to and from the DTE 108. Data is forwarded to and received from the UART 204, via the first output port 248 and the first input port 246, respectively.

Referring to FIG. 3, as an initialisation routine, the generator 206 disables the receive clock signal, and the transmit clock signal is set to a speed which is a multiple corresponding to sixteen times the last known successful autobaud rate (step 302). The transmit clock signal is allowed to run so that characters can be transmitted from the modem 102 to the interface 110 as normal. Additionally, the interrupt port 214 is enabled or unmasked, by the microcontroller 202.

When a command line 400 (FIG. 4) is transmitted from the DTE 108 via the interface cable 110 (FIG. 1) and received by the modem 102 at the second input port 252 of the transceiver 208, the command line 400, as described above, is prefixed with the ASCII characters 'A' and 'T' in accordance with the industry standard. The first character, namely 'A', comprises a start bit 406 having a leading edge 402. The command line 400 received by the transceiver 208 is transmitted to the UART 204, the single bit port 212 and the interrupt port 214, via the data bus 244.

The microcontroller 202 monitors the data bus 244 via the interrupt port 214 until the leading edge 402 of the command line 400 is detected (step 304) causing an interrupt. If the leading edge 402 is not detected, the microcontroller 202 continues to monitor the data bus 244 until the leading edge 402 is detected.

When the leading edge 402 is detected, the interrupt generated causes the microcontroller 202 to generate a logical HIGH signal at the reset counter terminal 216 so as to instruct the generator 206 to reset the counter. The generator 206 also generates the receiver clock signal 500 (FIG. 5) at a maximum speed (step 306) which, in this example, is a multiple corresponding to sixteen times the maximum autobaud rate. The UART 204, by virtue of the design of the UART 204, assumes that a data bit has been received after 16 clock cycles. However, once the receive clock signal has run at the maximum speed for sixteen cycles 502 (step 308), the UART 204 is tricked into believing that the start bit has been clocked into the UART 204, and the generator 206 ceases to generate 504 the receive clock signal 500 (step 310). However, this is not the case and the start bit is still being received from the transceiver 208. The microcontroller 202 then monitors the data bus 244 in order to detect a trailing edge 404 of the start bit (step 312) which is still being received. When the trailing edge 404 has been detected, the counter is locked by means of a locking signal generated by the microcontroller 202 at the control bus port 210. It should be noted that although the counter is locked, it is not essential to lock the counter and the counter can be read by the microcontroller 202 without the need to be locked first.

The counter value is then used by the generator 206 to select an appropriate division of the master clock rate to set the receive clock signal to a correct speed 506 for clocking the UART 204 (step 314). The interrupt is then masked and the remainder of the command line 400 is then clocked into the UART 204. Once the command line 400 has been completely read (step 316), the receiver clock signal is turned off and the transmit clock signal is set to the last successful autobaud rate as described above, i.e. the receive clock signal speed, to receive a subsequent command line (step 302). Also, the interrupt is unmasked again in order to receive a subsequent command line.

Although the above invention has been described in the context of a fixed wire telephone, it is not intended that the invention be limited to such systems and it is envisaged that other systems can be included, for example, a cellular telephone system.

Integration of the above described apparatus and method into a cellular telephone environment can simply be achieved by using a Communicate Atlas Ranger modem as the modem 102 and a Motorola 2700 transceiver as the network interface 104 and the network 100 can be implemented using a radio frequency medium.

In the above described example, it is possible to autobaud within a range from 300 bits per second to 115200 bits per second. However, it should be noted that the above technique does not have any limit to the speeds at which autobauding takes place and that the above range is only exemplary in relation to the above described implementation.

Claims

1. An apparatus for detecting a bit rate using a start bit, comprising a processor, communicating means coupled to the processor, a clock arranged to run at a speed greater than the bit rate, and a counter for determining the width of the start bit, the clock and the counter being coupled to the processor, wherein the processor is arranged to determine the bit rate using the speed of the clock and the width of the start bit.

2. An apparatus as claimed in Claim 1, wherein the communicating means is a universal asynchronous receiver transmitter.

3. An apparatus as claimed in Claim 1 or Claim 2, wherein the processor is arranged to detect a leading edge of the start bit.

4. An apparatus as claimed in any one of the preceding claims, wherein the processor is arranged to detect a trailing edge of the start bit.

5. An apparatus as claimed in any one of the preceding claims, wherein operation of the clock is selective.

6. An apparatus as claimed in any one of the preceding claims, wherein the counter is synchronised to the clock.

7. An apparatus as claimed in any one of the preceding claims, wherein the communicating means has a maximum bit rate and the clock is arranged to run a predetermined number of times faster than the maximum bit rate.

8. An apparatus as claimed in Claim 7, wherein the predetermined number of times is sixteen.

9. An apparatus as claimed in any one of the preceding claims, wherein the clock is arranged to run for a predetermined number of cycles.

10. An apparatus as claimed in Claim 9, wherein the predetermined number of cycles is sixteen.

11. An apparatus as claimed in any one of the preceding claims, wherein the clock is arranged to generate a transmit clock signal and a receive clock signal from a master clock signal.

12. An apparatus as claimed in Claim 11, wherein the receive clock signal is a factor of the master clock signal.

13. An apparatus as claimed in any one of the preceding claims, wherein the processor has a bit port for sensing data polarity.

14. An apparatus as claimed in any one of the preceding claims, the processor is arranged to generate an interrupt in response to the start bit.

15. An apparatus as claimed in any one of the preceding claims, wherein the receive clock signal is halted, the transmitter clock signal is enabled, and the clock and the counter are initialised.

16. An apparatus for detecting a bit rate using a start bit substantially as hereinbefore described with reference to FIG. 2, 4 and 5.

17. A method of detecting a bit rate using a start bit, comprising the steps of:

starting a clock and a counter in response to a characteristic of the start bit, the clock being arranged to run at a speed greater than the bit rate,

determining the width of the start bit using the counter,

determining the bit rate using the speed of the clock and the width of the start bit.

18. A method as claimed in Claim 17, wherein the characteristic of the start bit is a leading edge of the start bit.

19. A method as claimed in Claim 17 or Claim 18, further comprising running the clock a predetermined number of times faster than the bit rate.

20. A method as claimed in Claim 19, wherein the predetermined number of times is sixteen.

21. A method as claimed in any one of Claims 17 to 20, further comprising running the clock for a predetermined number of cycles.

22. A method as claimed in Claim 21, wherein the predetermined number of cycles is sixteen.

23. A method as claimed in any one of the Claims 17 to 22, further comprising generating a receive clock signal and a transmit clock signal from a master clock.

24. A method as claimed in any one of Claims 17 to 23, further comprising generating a processor interrupt in response to the start bit.

25. A method of detecting a bit rate using a start bit substantially as hereinbefore described with reference to FIG. 3.

The Patent Office

11

Application No:	GB 9708370.3	**Examiner:**	David Midgley
Claims searched:	1-25	**Date of search:**	8 July 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4P PDRX,PEM

Int Cl (Ed.6): H04L 25/02

Other: ONLINE:WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	WO 94/22252 A1	(ELSA) Whole doc.	1,17 at least
X	WO 92/02085 A1	(GENERAL) Whole doc.	"
X	US 5206888	(NEC) See, especially, col. 2, lines 40-60.	"
A	US 5072407	(GANDALF)	1,17
A	US 3909724	(ADDRESSOGRAPH)	"

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.